REMARKS

1. Introduction

In the Office Action mailed May 21, 2009, the Examiner rejected claims 1-3, 5, 7, and 27 under 35 U.S.C. § 102(b) as being anticipated by Chou et al., U.S. Pub. No. 2002/0042027 ("Chou").

The Examiner rejected claim 4 under 35 U.S.C. § 103(a) as being unpatentable over Chou in view of DePuydt et al., U.S. Patent No. 6,030,556 ("DePuydt").

The Examiner rejected claim 6 under 35 U.S.C. § 103(a) as being unpatentable over Chou in view of Chou, U.S. Patent No. 5,772,905 ("Chou '905").

The Examiner rejected claim 8 under 35 U.S.C. § 103(a) as being unpatentable over Chou in view of Kub et al., U.S. Patent No. 6,323,108 ("Kub").

In response, Applicant has amended claims 1 and 4, and Applicant has canceled claim 2. Claims 9-26 were previously canceled. Thus, claims 1, 3-8, and 27 are currently pending.

Applicant respectfully requests reconsideration and allowance of the claims, as amended herein, for the reasons set forth below.

2. Response to the claim rejections

Applicant has amended claim 1 to recite "a semiconductor or metal layer positioned on the polymer layer" and to specify that the texturing is caused "by induction of stress in the polymer layer with the semiconductor or metal layer present." These amendments are supported by Applicant's specification, for example, at page 2, lines 31-34 and page 6, lines 3-17.

Applicant submits that amended claim 1 is clearly allowable over Chou because Chou does not disclose a silicon or metal layer positioned on the polymer layer. In rejecting claim 2 (now cancelled), the Examiner stated that "[i]n addition to being a substrate, the wafer made of silicon, is a semiconductor." *See* Office Action, p. 2. But the "semiconductor or metal layer" recited in amended claim 1 is a different layer than the substrate, as claim 1 specifies that the single-phase polymer layer is positioned on the substrate and the semiconductor or metal layer is positioned on the polymer layer.

Moreover, Chou teaches away from a semiconductor or metal layer as recited in claim 1. In the Examiner's rationale for rejecting claim 1, the Examiner has treated the film 33 in Chou as corresponding to the claimed "single-phase polymer layer" and the pillars 49 that self-assemble in film 33 during a heat-and-cool cycle (with a mask 35 placed a certain distance above the surface of film 33) as corresponding to the claimed "textured surface." Applicant does not concede that the Examiner's correspondences are valid. However, even if these correspondences were to be accepted, Chou makes clear that the open space between film 33 and mask 35 is what enables the formation of pillars 49 in film 33:

> The open space between the initial PMMA film 33 and the mask 35 gives the PMMA film 33 freedom to deform three-dimensionally.

See paragraph [0036]. Thus, Chou teaches away from "a semiconductor or metal layer positioned on the polymer layer" and teaches away from "texturing ... by induction of stress in the polymer layer with the semiconductor or metal layer present," as recited in amended claim 1.

Accordingly, Applicant submits that claim 1, as amended, is allowable over Chou for at least the foregoing reasons. Applicant further submits that claims 3-8 and 27 are allowable for at least the reason that they depend from an allowable claim.

3. Conclusion

Applicant submits that the present application is in condition for allowance, and notice to that effect is hereby requested. Should the Examiner feel that further dialog would advance the subject application to issuance, the Examiner is invited to telephone the undersigned at any time at (312) 913-0001.

Respectfully submitted,

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By: Richard A. Machonkin

Richard A. Machonkin
Registration No. 41,962